GEETHANJALI COLLEGE OF ENGINEERING AND TECHNOLOGY (AUTONOMOUS)
Cheeryal (V), Keesara (M), R.R. Dist., - 50131, Telangana State

Department of Electronics and Communication Engineering

M.Tech Program in Embedded Systems

Vision

To impart quality technical education in Electronics and Communication Engineering emphasizing analysis, design/synthesis and evaluation of hardware/ embedded software, using various Electronic Design Automation (EDA) tools with accent on creativity, innovation and research thereby producing competent engineers who can meet global challenges with societal commitment.

Mission

- To impart quality education in fundamentals of basic sciences, mathematics, electronics and communication engineering through innovative teaching-learning processes.
- To facilitate Graduates define, design, and solve engineering problems in the field of Electronics and Communication Engineering using various Electronic Design Automation (EDA) tools.
- To encourage research culture among faculty and students thereby facilitating them to be creative and innovative through constant interaction with R & D organizations and Industry.
- To inculcate teamwork, imbibe leadership qualities, professional ethics and social responsibilities in students and faculty.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

I. To provide the necessary skills to meet the current and future industrial challenges in the field of Embedded Systems.
II. To provide the necessary skills to take up design of Embedded Systems.
III. To provide positive attitude for lifelong learning and skills for effective communication so that the students can take up research and development work in the field of Embedded Systems.

PROGRAM OUTCOMES (POs)

1. Able to design, execution and evaluation of experiments on embedded platforms.
2. Able to design, analyze, and testing of systems that include both hardware and software.
3. Able to apply knowledge from the program and other disciplines to identify, formulate, solve novel advanced electronics engineering problems

4. Able to understand and integrate new knowledge within the field.
5. Able to apply advanced technical knowledge in multiple contexts
6. Able to understand and design advanced electronics systems (Analog and Digital Systems) and conduct experiments, analyze and interpret data.
7. Able to convey technical material through formal written reports which satisfy accepted standards of writing style.
8. Able to demonstrate effective communication skills in oral, written and electronic media.
9. Able to become knowledgeable about contemporary developments in the field of Embedded Systems.
10. Continue to improve their professional skills through lifelong learning

ACADEMIC REGULATIONS 2016 for CBCS Based M.Tech. (Regular) Programmes

(Effective for the students admitted into I year from the Academic Year **2016-17** onwards)

1.0 Post-Graduate Degree (M. Tech) Programmes in Engineering

GCET offers 2 Year (4 Semesters) full-time Master of Technology (M.Tech.) Degree programmes, under Choice Based Credit System (CBCS) at GCET Hyderabad with effect from the Academic Year 2016 - 17 onwards in the different branches of Engineering with different specializations.

2.0 Eligibility for Admission:

2.1 Admission to the M. Tech programme shall be made either on the basis of the Rank/Percentile earned by the candidate in the relevant qualifying GATE Examination / the Merit Rank obtained by the qualifying candidate at an Entrance Test conducted by the Telangana State Government (PGECET) for M.Tech. Programmes / an Entrance Test conducted by the Jawaharlal Nehru Technological University Hyderabad / on the basis of any other order of merit approved by the University, subject to reservations as prescribed by the Government from time to time.

2.2 The medium of instructions for all M. Tech programmes shall be ENGLISH only.

3.0 M.Tech. Programme Structure:

3.1 The M.Tech. Programmes of GCET are of Semester Pattern, with 4 Semesters constituting 2 Academic Years, each Academic Year having TWO Semesters (First/Odd and Second/Even Semesters). Each Semester shall be of 21 Weeks duration (inclusive of Examinations), with a minimum of 90 Instructional Days per Semester.

3.2 UGC/ AICTE specified Definitions/ Descriptions are adopted appropriately for various terms and abbreviations used in these M. Tech Programmes - Academic Regulations.

3.2.1 **Semester Scheme:**

Each Semester having - 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) as denoted are taken as 'references' for the present set of Regulations. The terms 'SUBJECT' or 'COURSE' imply the same meaning here, and refer to 'Theory Subject', or 'Lab Course', or 'Design/ Drawing Subject', or 'Seminar', or 'Comprehensive Viva', or 'Project', as the case may be.

3.2.2 **Credit Courses:**

All Subjects (or Courses) are to be registered by a student in a Semester to earn Credits. Credits shall be assigned to each Subject/ Course in a L: T: P: C (Lecture Periods: Tutorial Periods: Practicals Periods : Credits) Structure, based on the following general pattern …

• One hour/ Week/ Semester for Theory/ Lecture (L) Courses; and,

• Two hours/ Week/ Semester for Laboratory/ Practical (P) Courses or Tutorials (T).

Other student activities like Study Tour, Guest Lecture, Conference/ Workshop Participations, Technical Paper Presentations etc., and identified Mandatory Courses if any, will not carry Credits.

3.2.3 **Subject/ Course Classification:**

All Subjects/ Courses offered for the M. TECH are broadly classified as : (a) Core Courses (CoC), and (b) Elective Courses (EℓC).

- Core Courses (CoC) and Elective Courses (EℓC) are categorized as PS (Professional Subjects), which are further subdivided as – (i) PC (Professional/ Departmental Core) Subjects, (ii) PE (Professional/ Departmental Electives) , (iii) Seminar, (iv) Comprehensive Viva, and (v) Project Work (PW).

3.2.4 **Course Nomenclature:**

The Curriculum Nomenclature or Course-Structure Grouping for the M.Tech. Degree Programmes is as listed below …

S.No	***Broad Course Classification***	***Course Group/ Category***	***Courses Description***	***Credits***
1	Core courses (CoC)	PC-Professional core	Includes core subjects related to the Parent Discipline/ Department/ Branch of Engg.	20
2	Elective Courses (EℓC)	PE– Professional Electives	Includes Elective subjects related to the Parent Discipline/ Department/ Branch of Engg.	32
3	Core Courses	Project Work	M.Tech. Project or PG Project or PG Major Project	30
		Seminar	Seminar/ Colloquium based on core contents related to Parent Discipline/ Department/ Branch of Engg.	2
		Comprehensive Viva-voce	Viva-voce covering all the PG Subjects and related aspects	4
		Communication Skills/ Soft Skills	Lab oriented	2
Total Credits				**90**

4.0 Course Work:

4.1 A Student, after securing admission, shall pursue and complete the M.Tech. M. TECH in a minimum period of 2 Academic Years (4 Semesters), and within a maximum period of 4 Academic Years (starting from the Date of Commencement of I Year).

4.2 Each student shall Register for and Secure the specified number of Credits required for the completion of the M. Tech programme and Award of the M.Tech. Degree in respective Branch of Engineering with the chosen Specialization.
4.3 I Year is structured to provide typically 28 Credits (28 C) in each of the I and II Semesters, and II Year comprises of 34 Credits (34 C), totaling to 90 Credits (90 C) for the entire M.Tech. Programme.

5.0 Course Registration:

5.1 A 'Faculty Advisor' shall be assigned to each M.Tech. Programme with respective Specialization, who will advise the Students about the M.Tech. Programme Specialization, its Course Structure and Curriculum, Choice/ Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.
5.2 A Student may be permitted to Register for Subjects/ Courses of 'his CHOICE' with a typical total of 28 Credits per Semester in I Year (Minimum being 24 C and Maximum being 32 C, permitted deviation being ± 15%), and 16 Credits (inclusive of Project) per III Semester in II Year (Minimum being 16 C and Maximum being 32 C), 18 credits (inclusive of Project) per IV Semester in II Year (minimum being 18 C and maximum 32 C), based on his interest, competence, progress, and 'PRE-REQUISITES' as indicated for various Subjects/ Courses, in the Department Course Structure (for the relevant Specialization) and Syllabus contents for various Subjects/ Courses.
5.3 Choice for 'additional Subjects/ Courses' in any Semester (above the typical 28/16/18 Credit norm, and within the Maximum Permissible Limit of 32/32 Credits, during I/ II Years as applicable) must be clearly indicated in the Registration, which needs the specific approval and signature of the Faculty Advisor/ Counselor on hard-copy.
5.4 Dropping of Subjects/ Courses in any Semester of I Year may be permitted, ONLY AFTER obtaining prior approval and signature from the Faculty Advisor (subject to retaining a minimum of 24 Credits), 'within 15 Days of Time' from the beginning of the current Semester.

6.0 Attendance Requirements:

6.1 A Student shall be eligible to appear for the End Semester Examination (SEE) of any Subject, if he acquires a minimum of 75% of attendance in that Subject for that Semester.
6.2 A Student's Seminar Report and Seminar Presentation shall be eligible for evaluation, only if he ensures a minimum of 75% of his attendance in Seminar Presentation Classes during that Semester.
6.3 Condoning of shortage of attendance up to 10% (65% and above, and below 75%) in each Subject or Seminar of a Semester may be granted by the College Academic Council on genuine and valid grounds, based on the Student's representation with supporting evidence.
6.4 A stipulated fee per Subject/Seminar shall be payable towards condoning of shortage of attendance.
6.5 Shortage of Attendance below 65% in any Subject/Seminar shall in NO case be condoned.
6.6 A Student, whose shortage of attendance is not condoned in any Subject(s) or Seminar in any Semester, is considered as 'Detained in that Subject(s)/Seminar', and is not eligible to take

End Examination(s) of such Subject(s) (and in case of Seminars, his Seminar Report or Presentation are not eligible for evaluation) in that Semester; and he has to seek Re-registration for those Subject(s)/Seminar in subsequent Semesters, and attend the same as and when offered.

7.0 Academic Requirements:

The following Academic Requirements have to be satisfied, in addition to the Attendance Requirements mentioned in Item No. 6**.**

7.1 A Student shall be deemed to have satisfied the Academic Requirements and earned the Credits allotted to each Subject/ Course, if he secures not less than 40% Marks (28 out of 70 Marks) in the End Semester Examination, and a minimum of 50% of Marks in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades, this implies securing B Grade or above in that Subject.

7.2 A Student shall be deemed to have satisfied the Academic Requirements and earned the Credits allotted to - Seminar, and Comprehensive Viva-voce, if he secures not less than 50% of the total marks to be awarded for each. The Student would be treated as failed, if he - (i) does not attend the

Comprehensive Viva-voce as per the schedule given, or (ii) does not present the Seminar as required, or (ii) secures less than 50% of Marks (< 50 Marks) in Seminar/ Comprehensive Viva-voce evaluations. He may reappear for comprehensive viva where it is scheduled again; For seminar, he has to reappear in the next subsequent Semesters, as and when scheduled.

7.3 A Student shall - register for all Subjects covering 90 Credits as specified and listed in the Course Structure for the chosen M. TECH Specialization, put up all the Attendance and Academic requirements for securing 90 Credits obtaining a minimum of B Grade or above in each Subject, and 'earn all 90 Credits securing SGPA $\geq$ 5.0 (in each Semester) and final CGPA (ie., CGPA at the end of M. TECH) $\geq$ 5.0, to successfully complete the M. TECH.

7.4 Marks and Letter Grades obtained in all those Subjects covering the above specified 90 Credits alone shall be considered for the calculation of final CGPA, which shall be indicated in the Grade Card of II Year II Semester.

7.5 If a student registers for some more 'extra Subjects' (in the parent Department or other Departments/Branches of Engg.) other than those listed Subjects totaling to 90 Credits as specified in the Course Structure, the performances in those 'extra Subjects' (although evaluated and graded using the same procedure as that of the required 90 Credits) will not be taken into account while calculating the SGPA and CGPA. For such 'extra Subjects' registered, % marks and Letter Grade alone will be indicated in the Grade Card, as a performance measure, subject to completion of the Attendance and Academic Requirements as stated in Items 6 and 7.1 – 7.4 above.

7.6 Students who fail to earn 90 Credits as per the specified Course Structure, and as indicated above, within 4 Academic Years from the Date of Commencement of their I Year, shall forfeit their seats in M.Tech. Programme and their admissions shall stand cancelled.

7.7 When a Student is detained due to shortage of attendance in any Subject(s)/Seminar in any Semester, no Grade Allotment will be done for such Subject(s)/Seminar, and SGPA/ CGPA calculations of that Semester will not include the performance evaluations of such Subject(s)/Seminar in which he got detained. However, he becomes eligible for re-registration of such Subject(s)/Seminar (in which he got detained) in the subsequent Semester(s), as and when next offered, with the Academic Regulations of the Batch into which he gets readmitted, by paying the stipulated fees per Subject. In all these re-registration cases, the Student shall have to secure a fresh set of Internal Marks (CIE) and End Semester Examination Marks (SEE) for

performance evaluation in such Subject(s), and subsequent SGPA/ CGPA calculations.

7.8 A Student eligible to appear in the End Semester Examination in any Subject, but absent at it or failed (failing to secure B Grade or above), may reappear for that Subject at the supplementary examination (SEE) as and when conducted. In such cases, his Internal Marks (CIE) assessed earlier for that Subject/ Course will be carried over, and added to the marks to be obtained in the supplementary examination (SEE), for evaluating his performance in that Subject.

8.0 Evaluation - Distribution and Weightage of Marks:

8.1 The performance of a Student in each Semester shall be evaluated Subject-wise (irrespective of Credits assigned) with a maximum of 100 Marks for Theory or Practicals or Seminar or Drawing/Design or Comprehensive Viva-voce etc;

however, the M.Tech. Project Work (Major Project) will be evaluated for 200 Marks.

8.2 a) For Theory Subjects, CIE Marks shall comprise of - Mid-Term Examination Marks (for 25 Marks), and Assignment Marks (for 5 Marks).

b) During the Semester, there shall be 2 Mid-Term examinations. Each Mid-Term examination shall be for 25 Marks (with 120 minutes duration). The AVERAGE performance out of these two Mid-Term Examinations shall be considered for the award of 25 Marks.

8.3 For Practical Subjects, there shall be a Continuous Internal Evaluation (CIE) during the Semester for 30 Internal Marks, and 70 Marks are assigned for Lab./Practicals End Semester Examination (SEE). Out of the 30 Marks for Internals, day-to-day work assessment in the laboratory shall be evaluated for 20 Marks; and the performance in an internal Lab./Practical Test shall be evaluated for 10 marks. The SEE for Lab./ Practicals shall be conducted at the end of the Semester by the concerned Lab. Teacher and another faculty member of the same Department as assigned by the Head of the Department.

8.4 There shall be a Seminar Presentation in I Year I Semester or II Semester.

For the Seminar, the Student shall collect the information on a specialized topic, prepare a Technical Report and submit to the Department at the time of Seminar Presentation. The Seminar Presentation (along with the Technical Report) shall be evaluated by Two Faculty Members assigned by Head of the Department, for 100 Marks. There shall be no SEE or External Examination for Seminar.

8.5 Each Student shall appear for a Comprehensive Viva-Voce at the end of the III Semester (II Year I Semester). The Comprehensive Viva-Voce shall be conducted by a Committee, consisting of three senior faculty members of Department nominated by the Head of the Department, and the performance evaluation shall be for 100 Marks. There are no Internal Marks for the Comprehensive Viva-voce.

8.6 a) Every Student shall be required to execute his M.Tech. Project, under the guidance of the Supervisor assigned to him by the Head of Department. The Project shall start immediately after the completion of the I Year II Semester, and shall continue through II Year I and II Semesters. The Student shall carry out the literature survey, select an appropriate topic and submit a Project Proposal within 6 weeks (immediately after his I Year II Semester End Examinations), for approval by the Project Review Committee (PRC). The PRC shall be constituted by the Head of Department, and shall consist of the Head of Department, Project Supervisor, and a Senior Faculty Member of the Department. The Student shall present his Project Work Proposal to the PRC (PRC-I Presentation), on whose approval he can 'REGISTER for the PG Project'. Every Student must compulsorily register for his M.Tech. Project Work, within the 6 weeks of time-frame as specified above. After Registration, the Student shall carry out his work, and continually submit 'a fortnightly progress report' to his Supervisor throughout the Project period. The PRC will monitor the progress of the Project Work and review, through PRC-II and PRC-III Presentations – one at the end of the II Year I Semester, and one before the submission of
M.Tech. Project Work Report/ Dissertation.

b) After PRC-III presentation, the PRC shall evaluate the entire performance of the Student and declare the Project Report as 'Satisfactory' or 'Unsatisfactory'. Every Project Work Report/ Dissertation (that has been declared 'satisfactory') shall undergo 'Plagiarism Check' as per the
University/ College norms to ensure content plagiarism below a specified level of 30%, and to become acceptable for submission. In case of unacceptable plagiarism levels, the student shall resubmit the Project Work Report, after carrying out the necessary modifications/ additions to his Project Work/ Report as per his Supervisor's advice, within the specified time, as
suggested by the PRC.

c) If any Student could not be present for PRC-II at the scheduled time (after approval and registration of his Project Work at PRC-I), his submission and presentation at the PRC-III time (or at any other PRC specified dates) may be treated as PRC-II performance evaluation, and delayed PRC-III dates for him may be considered as per PRC recommendations. Any Student is allowed to submit his M.Tech. Project Dissertation 'only after completion of 40 weeks from the date of approval/registration' of his Project, and after obtaining all approvals from the PRC.

d) A total of 200 Marks are allotted for the M.Tech. Project Work, (out of which 100 Marks are allotted for internal evaluation and 100 Marks for external evaluation). For internal Evaluation of 100 marks, Project Supervisor shall evaluate for 60 marks based on the

continuous Internal Evaluation(CIE) of the student's performance and combined PRC-I, II & III performance evaluation will be for 40 marks (to be awarded by PRC, as SEE).

8.7 a) The Student shall be allowed to submit his Project Dissertation, only on the successful completion of all the prescribed PG Subjects (Theory and Labs.), Seminar, Comprehensive Viva-voce etc. (securing B Grade or above), and after obtaining all approvals from PRC. In such cases, the M.Tech. Dissertations will be sent to an External Examiner nominated by the Principal of the College, on whose 'approval', the Student can appear for the M.Tech. Project Viva-voce Examination, which shall be conducted by a Board, consisting of the PG Project Supervisor, Head of the Department, and the External Examiner who adjudicated the M.Tech. Project Work and Dissertation. The Board shall jointly declare the Project Work Performance as 'satisfactory', or 'unsatisfactory'; and in successful cases, the External Examiner shall evaluate the Student's Project Work presentation and performance for 100 Marks (SEE).

b) If the adjudication report of the External Examiner is 'not favourable' , then the Student shall revise and resubmit his Dissertation after one Semester, or as per the time specified by the External Examiner and/ or the PRC. If the resubmitted report is again evaluated by the External Examiner as 'not favourable', then that Dissertation will be summarily rejected. Subsequent actions for such Dissertations may be considered, only on the specific recommendations of the External Examiner and/ or PRC.

c) In cases, where the Board declared the Project Work Performance as 'unsatisfactory', the Student is deemed to have failed in the Project Vivavoce Examination, and he has to reappear for the Viva-voce Examination as per the Board recommendations. If he fails in the second Viva-voce Examination also, he will not be considered eligible for the Award of the Degree, unless he is asked to revise and resubmit his Project Work by the Board within a specified time period (within 4 years from the date of commencement of his I Year I Semester).

9.0 Re-Admission / Re-Registration:

9.1 **Re-Admission for Discontinued Students:**

Students, who have discontinued the M.Tech. Degree Programme due to any reasons what so ever, may be considered for 'Readmission' into the same Degree Programme (with same specialization) with the Academic Regulations of the Batch into which he gets readmitted, with prior permission from the concerned authorities, subject to Item 4.1.

9.2 Re-Registration for Detained Students:

When any Student is detained in a Subject (s)/ Seminar due to shortage of attendance in any Semester, he may be permitted to re-register for the same Subject in the 'same category' (Core or Elective Group) or equivalent Subject if the same Subject is not available, as suggested by the Board of Studies of that Department, as when offered in the sub-sequent Semester(s), with the Academic Regulations of the Batch into which he seeks re-registration , with prior permission from the concerned authorities, subject to Item 4.1.

10.0 Grading Procedure:

10.1 Marks will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Seminar, or Project, etc., based on the % marks obtained in CIE

+ SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 6 above, and a corresponding Letter Grade shall be given.

10.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	*Letter Grade (UGC Guidelines)*	*Grade Points*
80% and above (≥ 80% , ≤ 100%)	O (Outstanding)	10
Below 80% but not less than 70% (≥ 70% , < 80%)	A^+ (Excellent)	9
Below 70% but not less than 60% (≥ 60% , < 70%)	A (Very Good)	8
Below 60% but not less than 55% (≥ 55% , < 60%)	B^+ (Good)	7
Below 55% but not less than 50% (≥ 50% , < 55%)	B (above Average)	6
Below 50% (< 50%)	F (Fail)	0
Absent	Ab	0

10.3 A student obtaining F Grade in any Subject shall be considered 'failed' and is be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIEMarks) in those Subjects will remain the same as those he obtained earlier.

10.4 A Letter Grade does not imply any specific % of Marks.

10.5 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course (excluding Mandatory non-credit Courses). Then the corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

10.6 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (ΣCP) secured from ALL Subjects/ Courses registered in a Semester,
by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

$$\text{SGPA} = \{ \sum_{i=1}^{N} C_i G_i \} / \{ \sum_{i=1}^{N} C_i \} \quad \text{.... For each Semester,}$$

where 'i' is the Subject indicator index (takes into account all Subjects in a Semester), 'N' is the no. of Subjects 'REGISTERED' for the Semester (as specifically required and listed under

the Course Structure of the parent Department), is the no. of Credits allotted to the ith Subject, and represents the Grade Points (GP) corresponding to the Letter Grade awarded for that ith Subject.

10.7 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters.

CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year second Semester onwards, at the end of each Semester, as per the formula

$$\mathbf{CGPA = \{ \sum_{j=1}^{M} C_j G_j \} / \{ \sum_{j=1}^{M} C_j \} \ldots \text{ for all S Semesters registered}}$$

(ie., upto and inclusive of S Semesters, S ≥ 1),

where 'M' is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' from the 1st Semester onwards upto and inclusive of the Semester S (obviously M > N), 'j' is the Subject indicator index (takes into account all Subjects from 1 to S Semesters), is the no. of Credits allotted to the jth Subject, and represents the Grade Points (GP) corresponding to the Letter Grade awarded for that jth Subject. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

10.8 For Merit Ranking or Comparison Purposes or any other listing, ONLY the 'ROUNDED OFF' values of the CGPAs will be used.

10.9 For Calculations listed in Item 10.5 – 10.8, performance in failed Subjects/ Courses (securing F Grade) will also be taken into account, and the Credits of such Subjects/Courses will also be included in the multiplications and summations. However, Mandatory Courses will not be taken into consideration.

10.10 A student shall be declared successful or 'passed' in a Semester, only when he gets a SGPA ≥ 5.00 (at the end of that particular Semester); and a student shall be declared successful or 'passed' in the entire M. TECH, only when gets a CGPA ≥ 5.00; subject to the condition that he secures a GP ≥ 6 (B Grade or above) in every registered Subject/ Course in each Semester (during the entire M. TECH) for the Degree Award, as required.

10.11 After the completion of each Semester, a Grade Card or Grade Sheet (or Transcript) shall be issued to all the Registered Students of that Semester, indicating the Letter Grades and Credits earned. It will show the details of the Courses Registered (Course Code, Title, No. of Credits, Grade Earned etc.), Credits earned, SGPA, and CGPA.

10.12 **Passing Standards :**

10.12.1 A Student shall be declared successful or 'passed' in a Semester, only when he gets a SGPA ≥ 5.00 (at the end of that particular Semester); and a Student shall be declared successful or 'passed' in the entire M. TECH, only when gets a CGPA ≥ 5.00; subject to the condition that he secures a GP ≥ 6 (B Grade or above) in every registered Subject/ Course in each Semester (during the entire M. TECH), for the Award of the Degree, as required.

10.12.2 After the completion of each Semester, a Grade Card or Grade Sheet (or Transcript) shall be issued to all the Registered Students of that Semester, indicating the Letter Grades and Credits earned. It will show the details of the Courses Registered (Course Code, Title, No. Of Credits, Grade Earned), Credits earned, SGPA, and CGPA etc.

11.0 Declaration of Results:

11.1 Computation of SGPA and CGPA are done using the procedure listed in 10.5 – 10.8.

11.2 For Final % of Marks equivalent to the computed CGPA, the following formula may be used ..

% of Marks = (CGPA – 0.5) x 10

12.0 Award of Degree and Class:

12.1 A Student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (M. TECH), and secures the required number of **90** Credits (with GP ≥ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

12.2 **Award of Class**

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following four classes based on the % CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	6.75 ≤ CGPA < 7.75
Second Class	5.75 ≤ CGPA < 6.75
Pass Class	5.0 ≤ CGPA < 5.75

12.3 A student with final CGPA (at the end of the M. TECH) < 5.00 will not be eligible for the Award of Degree.

13.0 Withholding of Results:

13.1 If a Student has not paid fees to University/ College at any stage, or has pending dues against his name due to any reason whatsoever, or if any case of indiscipline is pending against him, the result of the Student may be withheld, and he will not be allowed to go into the next higher Semester.

The Award or issue of the Degree may also be withheld in such cases.

14.0 Transitory Regulations:

14.1 A Student - who has discontinued for any reason, or who has been detained for want of attendance as specified, or who has failed after having undergone M. TECH, may be considered eligible for readmission to the same M. TECH with same set of Subjects/ Courses (or equivalent Subjects/ Courses as the case may be), and same Professional Electives (or from

same set/category of Electives or equivalents as suggested), as and when they are offered (within the timeframe of 4 years from the Date of Commencement of his I Year I Semester).

15.0 Student Transfers:

15.1 There shall be no Branch/ Specialization transfers after the completion of Admission Process.

16.0 Scope:

i) Where the words "he", "him", "his", occur in the write-up of regulations, they include "she", "her", "hers".

ii) Where the words "Subject" or "Subjects", occur in these regulations, they also imply "Course" or "Courses".

iii) The Academic Regulations should be read as a whole, for the purpose of any interpretation.

iv) In case of any doubt or ambiguity in the interpretation of the above regulations, the decision of the Vice-Chancellor/ Principal is final.

v) The College may change or amend the Academic Regulations, and/ or Course Structure, and/ or Syllabi at any time, and the changes or amendments made shall be applicable to all Students with effect from the dates as notified by the University/ College

	Nature of Malpractices If the candidate:	**Punishment**
1 (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
1 (b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including

	of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to	Cancellation of the performance in that subject.

	award pass marks.	
6	Refuses to obey the orders of the Chief Superintendent / Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer- in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or	Expulsion from the examination hall and

	firearm in the examination hall.	cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further Action to award suitable punishment.	

18. GENERAL:

• **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

• **Credit Point:** It is the product of grade point and number of credits for a course.

• The Academic Regulations should be read as a whole for the purpose of any interpretation.

• The University/College reserves the right of altering the Academic Regulations and/or Syllabus/Course Structure, as and when necessary. The modifications or amendments may be applicable to all the candidates on rolls, as specified by the University/College.

• Wherever the words 'he' or 'him' or 'his' occur in the above regulations, they will also include 'she' or 'her' or 'hers'.

• Wherever the word 'Subject' occurs in the above regulations, it implies the 'Theory Subject', 'Practical Subject' or 'Lab.' and 'Seminar'.

• In case of any ambiguity or doubt in the interpretations of the above regulations, the decision of the Principal shall be final.

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GEETHANJALI COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)
SCHEME OF INSTRUCTION AND EXAMINATION
M.Tech. (Embedded Systems)

Academic Regulations: AR-16 **Academic Year 2016-17**

PROGRAM STRUCTURE

I Year - I SEMESTER

Course Code	Course	L	T	P	Evaluation			Credits
					CIE	SEE	TOT	
16MES101	Embedded Systems Design	**4**	**-**	**-**	**30**	**70**	**100**	**4**
16MES102	Digital Control Systems	**4**	**-**	**-**	**30**	**70**	**100**	**4**
	Elective-I							
16MES103	Digital System Design with PLDs	**4**	**-**	**-**	**30**	**70**	**100**	**4**
16MES104	Advanced Data Communications							
16MES105	Advanced Digital Signal Processing							
	Elective-II							
16MES106	VLSI Technology and Design	**4**	**-**	**-**	**30**	**70**	**100**	**4**
16MES107	Coding Theory and Techniques							
16MES108	Speech and Audio Signal Processing							
	Elective-III							
16MES109	Reliability Engineering	**4**	**-**	**-**	**30**	**70**	**100**	**4**
16MES110	Intelligent Control							
16MES111	Sensors and Actuators							
	Elective-IV							
16MES112	Embedded Real Time Operating Systems	**4**	**-**	**-**	**30**	**70**	**100**	**4**
16MES113	Advanced Computer Architecture							
16MES114	Scripting Languages.							
	SEMINAR/ LAB							
16MES1S1	Seminar	**-**	**-**	**4**	**100**	**-**	**100**	**2**
16MES1L1	Embedded Systems Lab	**-**	**-**	**4**	**30**	**70**	**100**	**2**
	Total	**24**	**-**	**8**	**310**	**490**	**800**	**28**

I Year - II SEMESTER

Course Code	Course	L	T	P	Evaluation			Credits
					CIE	SEE	TOT	
16MES201	System on Chip Architecture	**4**	**-**	**-**	**30**	**70**	**100**	**4**
16MES202	Embedded Programming	**4**	**-**	**-**	**30**	**70**	**100**	**4**
	Elective-V							
16MES203	Design of Fault Tolerant Systems	**4**	**-**	**-**	**30**	**70**	**100**	**4**
16MES204	Embedded Networks							
16MES205	Image and Video processing							
	Elective-VI							
16MES206	Hardware - Software Co-Design	**4**	**-**	**-**	**30**	**70**	**100**	**4**
16MES207	Ad-hoc and Wireless Sensor Networks							
16MES208	Digital Signal Processors and Controllers							
	Elective-VII							
16MES209	Modern Control Theory	**4**	**-**	**-**	**30**	**70**	**100**	**4**
16MES210	Optimization Techniques							
16MES211	Robotics							
	Elective-VIII							
16MES212	Network Security and Cryptography	**4**	**-**	**-**	**30**	**70**	**100**	**4**
16MES213	Mobile Computing							
16MES214	High Speed Networks							
	LAB							
16MES2L1	Embedded Programming Laboratory	**-**	**-**	**4**	**30**	**70**	**100**	**2**
16MES2S1	Soft Skills	**-**	**-**	**4**	**100**	**-**	**100**	**2**
	Total	**24**	**-**	**8**	**310**	**490**	**800**	**28**

II Year –I Semester								
Course Code	**Course**	**L**	**T**	**P**	**Evaluation**			**Credits**
					CIE	**SEE**	**TOT**	
16MES3C1	Comprehensive Viva-Voce	**-**	**-**	**-**	**-**	**100**	**100**	**4**
16MES3P1	Project Phase –I	**-**	**-**	**-**	**-**	**-**	**-**	**12***
	Total Credits							**16**

II Year –II Semester								
Course Code	**Course**	**L**	**T**	**P**	**Evaluation**			**Credits**
					CIE	**SEE**	**TOT**	
16MES4P1	Project Phase-II & Dissertation	**-**	**-**	**-**	**100**	**100**	**200**	**18***
	Total credits							**18**

*Credits will be awarded only at the end of Semester End Examination (SEE). Marks Memo for project shall be generated only after successful completion of the project.

Academic Year 2016-17

16MES101-EMBEDDED SYSTEMS DESIGN

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem

Prerequisite: Microprocessor and Microcontrollers

Course Objectives:

1. To provide an overview of Design Principles of Embedded System.
2. To provide clear understanding about the role of firmware , operating systems in correlation with hardware systems.

Course Outcomes:

1. Expected to understand the selection procedure of Processors in the Embedded domain.
2. Design Procedure for Embedded Firmware.
3. Expected to visualize the role of Real time Operating Systems in Embedded Systems
4. Expected to evaluate the Correlation between task synchronization and latency issues

UNIT -I: Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II: Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III: Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV: RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V: Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.
2. Embedded Systems - Raj Kamal, TMH.

REFERENCE BOOKS:

1. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
2. Embedded Systems – Lyla, Pearson, 2013
3. An Embedded Software Primer - David E. Simon, Pearson

Academic Year 2016-17

16MES102- DIGITAL CONTROL SYSTEMS

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem

Prerequisite: Control Systems

Course Objectives:

1. To explain basic and digital control system for the real time analysis and design of control systems.
2. To apply the knowledge state variable analysis in the design of discrete systems.
3. To explain the concept of stability analysis and design of discrete time systems.

Course Outcomes: Upon the completion of this course, the student will be able to

1. Apply the concepts of Digital control systems.
2. Analyze and design of discrete systems in state variable analysis.
3. To relate the concepts of stability analysis and design of discrete time systems.

UNIT – I: Concept & Representation of Discrete time Systems: Block Diagram of typical control system- advantages of sampling in control systems – examples of discrete data and digital systems – data conversion and quantization – sample and hold devices – D/A and A/D conversion – sampling theorem – reconstruction of sampled signals.
Z- transform: Definition of Z -transforms – mapping between s-plane and z-plane – inverse z- transform – properties of z-transforms - ROC of z-transforms –pulse transfer function – relation between G(s) and G(z) – signal flow graph method applied to digital control systems.

UNIT- II: State Space Analysis: State space modeling of discrete time systems – state transition equation of discrete time invariant systems – solution of time invariant discrete state equations: recursive method and the Z-Transformation method – conversion of pulse transfer function to the state model & vice-versa – Eigen values – Eigen vectors of discrete time system-matrix (A) – Realization of pulse transformation in state space form, discretization of continuous time systems, Computation of state transition matrix and its properties. Response of sample data system between sampling instants.

UNIT – III: Controllability, Observability & Stability tests: Concept of controllability, stabilizability, observability and reachability - Controllability and observability tests, Transformation of discrete time systems into controllable and observable forms.Stability: Definition of stability – stability tests – The second method of Liapunov.

UNIT- IV: Design of discrete time Controllers and observers: Design of discrete time controller with bilinear transformation – Realizatiion of digital PID controller-Design of deadbeat controller; Pole placement through state feedback.

UNIT-V: State Observers: Design of - Full order and reduced order observers. Study of observer based control design.

TEXT BOOKS:

1. K. Ogata , Discrete-Time Control systems, Pearson Education/PHI, 2nd Edition.
2. V. I. George, C. P. Kurian, Digital Control Systems, Cengage Learning.

REFERENCES:

1. M.Gopal, Digital Control Engineering, New Age Int. Pvt. Ltd., 2014
2. Kuo, Digital Control Systems, Oxford University Press, 2nd Edition, 2003.
3. M.Gopal , Digital Control and State Variable Methods, TMH.
4. M. Sami Fadali Antonio Visioli, Digital Control Engineering Analysis and Design, Academic Press

Academic Year 2016-17

16MES103-DIGITAL SYSTEM DESIGN WITH PLDs
(Elective – I)

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem

Prerequisite: Switching Theory and Logic Design

Course Objectives:

1) To provide extended knowledge of digital logic circuits in the form of state model approach.
2) To provide an overview of system design approach using programmable logic devices.
3) To provide and understand of fault models and test methods.
4) To get exposed to the various architectural features of CPLDS and FPGAS.
5) To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6) To expose software tools used for design process with the help of case studies.

Course Outcomes:

1) To understands the minimization of Finite state machine.
2) To exposes the design approaches using ROM's, PAL's and PLA's.
3) To understands Fault models and test pattern generation techniques for fault detection.
4) To design fault diagnosis in sequential circuits.
5) To provide exposure to various CPLDS and FPGAS available in market.
6) To acquire knowledge in one hot state machine design applicable to FPGA.
7) To get exposure to EDA tools.
8) To provide understanding in the design of flow using case studies.

UNIT-I: Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs-Altera CPLDs, FPGAs -FPGA technology, architecture, virtex CLB and slice- Stratix LAB and ALM-RAM Blocks, DSP Blocks, Clock Management, I/O standards, Additional features.

UNIT-II: Analysis of clocked sequential circuits with state graphs and tables:
A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation.

UNIT-III: Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs,

Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design.

UNIT-IV: Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model. Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults.

UNIT-V: Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

TEXTBOOKS:

1. Fundamentals of Logic Design-Charles H.Roth,Jr. -5th Ed.,Cengage Learning.
2. Logic Design Theory-N.N.Biswas,PHI

REFERENCES:

1. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.
2. Digital Circuits and Logic Design-Samuel C.LEE,PHI 2008
3. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
4. Switching and Automata Theory, Z V Kohavi.

Academic Year 2016-17

16MES104- ADVANCED DATA COMMUNICATIONS
(Elective – I)

M.Tech. I Year I-Sem

L	T	P	C
4	-	-	4

Prerequisite: Digital Communications

Course Objectives:

1. To learn about basics of Data Communication networks, different protocols, standards and layering concepts.
2. To study about error detection and correction techniques.
3. Know about link layer protocol and point to point protocols.
4. To understand Medium Access Control sub layer protocols
5. To know about Switching circuits, Multiplexing and Spectrum Spreading techniques for data transmission.
6. To study Wired LANs different Ethernet standards

Course Outcomes: At the end of the course, the student will be able to:

1. Understand the concepts of Data Communication networks, different protocols, standards and layering.
2. Acquire the knowledge of error detection, forward and reverse error correction techniques.
3. Analyze link layer protocol and point to point protocols
4. Explain and compare the performance of different MAC protocols like Aloha, CSMA, CSMA/CA, TDMA, FDMA & CDMA.
5. Understand the features and the significance of Switching circuits, Multiplexing and Spectrum Spreading for data transmission.
6. Understand the characteristics of Wired LANs and also the operation and applications of Connecting Devices
7. Understand the services and functions of Network layer protocols.

Unit I: Data Communications and Layered Structures: Data Communications, Networks and Network Types, Internet History, Standards and Administration, Protocol Layering, TCP/IP protocol suite, OSI Model. Digital Data Transmission, DTE-DCE interface. **Data Link Layer:** Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol.

Unit II: Error Detection and Correction: Types of Errors, Redundancy, detection versus correction, Coding Block Coding: Error Detection, Vertical redundancy cheeks, longitudinal redundancy cheeks, Error Correction, Error correction single bit, Hamming code. **Cyclic Codes**: Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum
Data Link Control: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol

Unit III: Media Access Control (MAC) Sub Layer: Random Access, Aloha, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation, Polling-Token Passing, Channelization - Frequency Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA).

Unit IV: Switching: Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of switch. **Multiplexing and Spectrum Spreading:** Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing, Spread Spectrum - Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum.

Unit V: Wired LANS: Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Giga bit Ethernet. **Connecting Devices:** Hubs, Link Layer Switches, Routers
Networks Layer: Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic Host Configuration Protocol (DHCP), Network Address Resolution(NATF), Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches.

TEXT BOOKS:

1. Data Communications and Networking - B. A. Forouzan, 5th , 2013,TMH.
2. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.

REFERENCE BOOKS:

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data Communications and Computer Networks- Brijendra Singh, 2nd ed., 2005, PHI.

Academic Year 2016-17

16MES105- ADVANCED DIGITAL SIGNAL PROCESSING
(Elective – I)

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem

Prerequisite: Digital Signal Processing

Course Objectives:

The objectives of this course are to make the student

1. Understand the design of various types of digital filters and implement them using various implementation structures and study the advantages & disadvantages of a variety of design procedures and implementation structures.
2. understand the concept and need for Multi-rate signal Processing and their applications in various fields of Communication & Signal Processing
3. Understand difference between estimation & Computation of Power spectrum and the need for Power Spectrum estimation.
4. Study various Parametric & Non parametric methods of Power spectrum estimation techniques and their advantages & disadvantages
5. Understand the effects of finite word/register length used in hardware in implementation of various filters and transforms using finite precision processors.

Course Outcomes:

On completion of this course student will be able to

1. Design and implement a filter which is optimum for the given specifications.
2. Design a Multi-rate system for the needed sampling rate and can implement the same using Poly-phase filter structures of the needed order.
3. Estimate the power spectrum of signal corrupted by noise through a choice of estimation methods: Parametric or Non Parametric.
4. Can calculate the output Noise power of different filters due to various finite word length effects viz. ADC Quantization, product quantization, and can calculate the scaling factors needed to avoid Limit cycles: Zero input, overflow. Also they can decide the stability of the system by studying the effect due to coefficient quantization while implementing different filters and transforms.

UNIT –I: Review of DFT, FFT, IIR Filters and FIR Filters:

Introduction to filter structures (IIR & FIR).Implementation of Digital Filters, specifically 2^{nd} Order Narrow Band Filter and 1^{st} Order All Pass Filter. Frequency sampling structures of FIR, Lattice structures, Forward prediction error, Backward prediction error, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT -II: Non-Parametric Methods:
Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman-Tukey methods, Comparison of all Non-Parametric methods

UNIT - III: Parametric Methods:
Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation, Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

UNIT –IV: Multi Rate Signal Processing:
Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion. Examples of up-sampling using an All Pass Filter.

UNIT –V: Applications of Multi Rate Signal Processing:
Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Subband Coding of Speech Signals, Quadrature Mirror Filters, Transmultiplexers, Over Sampling A/D and D/A Conversion.

TEXT BOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications - J.G.Proakis& D. G. Manolakis, 4th Ed., PHI.
2. DSP – A Practical Approach – Emmanuel C. Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

REFERENCE BOOKS:

1. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
2. Modern spectral Estimation: Theory & Application – S. M .Kay, 1988, PHI.
3. Multi Rate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education.
4. Digital Signal Processing: A Practitioner's Approach, Kaluri V. Rangarao, Ranjan K. Mallik ISBN: 978-0-470-01769-2, 210 pages, November 2006 John Weley.
5. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

Academic Year 2016-17

16MES106- VLSI TECHNOLOGY AND DESIGN
(Elective – II)

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem

Prerequisite: VLSI , ICA

Course Objectives:

1) Students from other engineering background to get familiarize with large scale integration technology.
2) To expose fabrication methods, layout and design rules.
3) Learn methods to improve Digital VLSI system's performance.
4) To know about VLSI Design constraints.
5) Visualize CMOS Digital Chip Design.

Course Outcomes:

1) Review of FET fundamentals for VLSI design.
2) To acquires knowledge about stick diagrams and layouts.
3) Enable to design the subsystems based on VLSI concepts.

UNIT –I: Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II: Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. **Logic Gates & Layouts:** Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III: Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV: Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V: Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

Academic Year 2016-17

16MES107- CODINGTHEORY AND TECHNIQUES
(Elective - II)

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem

Prerequisite: Digital Communications

Course Objectives:

1. To acquire the knowledge in measurement of information and errors.
2. T study the generation of various code methods.
3. To study the various application of codes.

Course Outcomes:

1. Learning the measurement of information and errors.
2. Obtain knowledge in designing various codes like block codes, cyclic codes, convolution codes, turbo codes and space codes.

UNIT – I: Coding for Reliable Digital Transmission and storage:
Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.
Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error- Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - II: Cyclic Codes : Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT – III: Convolution Codes : Encoding of Convolution Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolution codes in ARQ system.

UNIT – IV: Turbo Codes: LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolution codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding.

UNIT - V: Space-Time Codes: Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti's schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing : General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

TEXT BOOKS:

1. Error Control Coding- Fundamentals and Applications –Shu Lin, Daniel J.Costello,Jr, Prentice Hall,
2. Error Correcting Coding Theory-Man Young Rhee- 1989, McGraw-Hill

REFERENCE BOOKS:

1. Digital Communications-Fundamental and Application - Bernard Sklar, PE.
2. Digital Communications- John G. Proakis, 5th ed., 2008, TMH.
3. Introduction to Error Control Codes-Salvatore Gravano-oxford
4. Error Correction Coding – Mathematical Methods and Algorithms – Todd K.Moon, 2006, Wiley India.
5. Information Theory, Coding and Cryptography – Ranjan Bose, 2nd Edition, 2009, TMH.

Academic Year 2016-17

16MES108- SPEECH AND AUDIO SIGNAL PROCESSING
(Elective – II)

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem

Prerequisite: Adaptive Signal Processing

Course Objectives: The objectives of this course are to make the student

1. Understand the anatomy and Physiology of Speech Production system and perception model and to design an electrical equivalent of Acoustic model for Speech Production.
2. To understand the articulatory and acoustic interpretation of various phonemes and their allophones.
3. To analyze the speech in time domain and extract various time domain parameters used for various applications like pitch extraction, end point detection, Speech Compression, Speech Synthesis etc.,
4. To study the concept of Homomorphic system and its use in extracting the vocal tract information from speech using Cepstrum.
5. To study various Speech Signal Processing applications viz. Speech Enhancement, Speech Recognition, Speaker Recognition.
6. To study various Audio coding techniques based on perceptual modeling of the human ear.

Course Outcomes: On completion of this course student will be able to

1. Model an electrical equivalent of Speech Production system.
2. Extract the LPC coefficients that can be used to Synthesize or compress the speech.
3. Design a Homomorphic Vocoder for coding and decoding of speech.
4. Enhance the speech and can design an Isolated word recognition system using HMM.
5. Can extract the features for Automatic speaker recognition system which can used for classification.
6. Can design basic audio coding methods for coding the audio signal.

Unit – I : Fundamentals of Digital Speech Processing:

Anatomy & Physiology of Speech Organs, The Process of Speech Production, The Acoustic theory of speech production- Uniform lossless tube model, effect of losses in vocal tract, effect of radiation at lips, Digital models for speech signals. **Perception** : Anatomical pathways from the Ear to the Perception of Sound, The Peripheral Auditory system, Hair Cell and Auditory Nerve Functions, Properties of the Auditory Nerve. Block schematics of the Peripheral Auditory system.

Unit – II : Time Domain models for Speech Processing:

Introduction – Window considerations, Short time energy, average magnitude, average zero crossing rate, Speech vs Silence discrimination using energy and zero crossing, pitch period

estimation using a parallel processing approach, the short time autocorrelation function, average magnitude difference function, pitch period estimation using the autocorrelation function.

Linear Predictive Coding (LPC) Analysis : Basic principles of Linear Predictive Analysis : The Autocorrelation Method, The Covariance method, Solution of LPC Equations : Cholesky Decomposition Solution for Covariance Method, Durbin's Recursive Solution for the Autocorrelation Equations, comparison between the methods of solution of the LPC Analysis Equations, Applications of LPC Parameters : Pitch Detection using LPC Parameters, Formant Analysis using LPC Parameters.

Unit – III : Homomorphic Speech Processing:

Introduction , Homomorphic Systems for Convolution : Properties of the Complex Cepstrum, Computational Considerations , The Complex Cepstrum of Speech, Pitch Detection , Formant Estimation, The Homomorphic Vocoder.

Speech Enhancement: Speech enhancement techniques : Single Microphone Approach, Spectral Subtraction, Enhancement by re-synthesis, Comb filter, Wiener filter, Multi Microphone Approach.

Unit – IV:

Automatic Speech Recognition:

Basic pattern recognition approaches, parametric representation of Speech, Evaluating the similarity of Speech patterns, Isolated digit Recognition System, Continuous word Recognition system. Elements of HMM, Training & Testing of Speech using HMM.

Automatic Speaker Recognition: Recognition techniques, Features that distinguish speakers, MFCC, delta MFCC, Speaker Recognition Systems: Speaker Verification System , Speaker Identification System, Performance Metrics.

Unit – V: Audio Coding:

Lossless Audio Coding, Lossy Audio coding, Psychoacoustics , ISO -MPEG-1 Audio coding , MPEG - 2 Audio coding, MPEG - 2 Advanced Audio Coding, MPEG - 4 Audio Coding.

TEXT BOOKS:

1. Digital Processing of Speech Signals - L.R. Rabiner and S. W. Schafer. Pearson Education.
2. Digital Audio Signal Processing – Udo Zolzer, 2nd Edition, Wiley.

REFENCE BOOKS:

1. Speech & Audio Signal Processing- Ben Gold & Nelson Morgan, 1st Ed., Wiley
2. Discrete Time Speech Signal Processing: Principles and Practice - Thomas F. Quateri, 1st Ed., PE.
3. Digital Processing of Speech Signals. L.R Rabinar and R W Jhaung, 1978, PHI.
4. Speech Communications: Human & Machine - Douglas O'Shaughnessy, 2nd Ed., EEE Press.

Academic Year 2016-17

16MES109- RELIABILITY ENGINEERING
(Elective- III)

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem

Prerequisite: None

Course Objectives:

1. To comprehend the concept of Reliability and Unreliability
2. Derive the expressions for probability of failure, Expected value and standard deviation of Binominal distribution, Poisson distribution, normal distribution and weibull distributions.
3. Formulating expressions for Reliability analysis of series-parallel and Non-series parallel systems
4. Deriving expressions for Time dependent and Limiting State Probabilities using Markov models.

Course Outcomes: Upon the completion of this course, the student will be able to

1. Apply fundamental knowledge of Reliability to modeling and analysis of series-parallel and Non-series parallel systems.
2. Solve some practical problems related with Generation, Transmission and Utilization of Electrical Energy.
3. Understand or become aware of various failures, causes of failures and remedies for failures in practical systems.

Unit I:

Rules for combining probabilities of events, Definition of Reliability. Significance of the terms appearing in the definition. Probability distributions: Random variables, probability density and distribution functions. Mathematical expectation, Binominal distribution, Poisson distribution, normal distribution, Weibull distribution.

Unit II:

Hazard rate, derivation of the reliability function in terms of the hazard rate. Failures: Causes of failures, types of failures (early failures, chance failures and wear-out failures) . Bath tub curve. Preventive and corrective maintenance. Modes of failure. Measures of reliability: mean time to failure and mean time between failures.

Unit III:

Classification of engineering systems: series, parallel and series-parallel systems- Expressions for the reliability of the basic configurations. Reliability evaluation of Non-series- parallel configurations: Decomposition, Path based and cutest based methods, Deduction of the Paths and cut sets from Event tree.

Unit IV:

Discrete Markov Chains: General modeling concepts, stochastic transitional probability matrix, time dependent probability evaluation and limiting state probability evaluation of one component repairable model. Absorbing states. **Continuous Markov Processes:** Modeling concepts, State space diagrams, Stochastic Transitional Probability Matrix, Evaluating time dependent and limiting state Probabilities of one component repairable model. Evaluation of Limiting state probabilities of two component repairable model.

UNIT-V:

Approximate system Reliability analysis of Series systems, parallel systems with two and more than two components, Network reduction techniques. Minimal cutest/failure mode approach.

TEXT BOOKS:

1. "Reliability evaluation of Engineering systems", Roy Billinton and Ronald N Allan, BS Publications.
2. "Reliability Engineering", Elsayed A. Elsayed, Prentice Hall Publications.

REFERENCES:

1. "Reliability Engineering: Theory and Practice", By Alessandro Birolini, Springer Publications.
2. "An Introduction to Reliability and Maintainability Engineering", Charles Ebeling, TMH Publications.
3. "Reliability Engineering", E. Balaguruswamy, TMH Publications.

Academic Year 2016-17

16MES110- INTELLIGENT CONTROL
(Elective-III)

M.Tech. I Year I-Sem

L	T	P	C
4	-	-	4

Prerequisite: None

Course Objectives:
1. Gaining an understanding of the functional operation of a variety of intelligent control techniques and their bio-foundations
2. The study of control-theoretic foundations
3. Learning analytical approaches to study properties

Course Outcomes:
Upon the completion of this course, the student will be able to
1. Develop Neural Networks, Fuzzy Logic and Genetic algorithms.
2. Implement soft computing to solve real-world problems mainly pertaining to control system applications

Unit-I
Introduction and motivation. Approaches to intelligent control. Architecture for intelligent control. Symbolic reasoning system, rule-based systems, the AI approach. Knowledge representation. Expert systems.

Unit-II
Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feedforward Multilayer Perceptron. Learning and Training the neural network. Data Processing: Scaling, Fourier transformation, principal-component analysis.

Unit-III
Networks: Hopfield network, Self-organizing network and Recurrent network. Neural Network based controller Case studies: Identification and control of linear and nonlinear dynamic systems using Matlab- Neural Network toolbox. Stability analysis of Neural-Network interconnection systems.

Unit-IV
Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters. Solution of typical control problems using genetic algorithm. Concept on some other search techniques like tabu search and ant-colony search techniques for solving optimization problems.

Unit-V
Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control. Fuzzification, inferencing and defuzzification. Fuzzy knowledge and rule bases. Fuzzy modeling and control schemes for

nonlinear systems. Fuzzy logic control for nonlinear time-delay system. Implementation of fuzzy logic controller using Matlab fuzzy-logic toolbox. Stability analysis of fuzzy control systems.

Text Books:

1. Simon Haykins, Neural Networks: A comprehensive Foundation, Pearson Edition, 2003.
2. T.J.Ross, Fuzzy logic with Fuzzy Applications, Mc Graw Hill Inc, 1997.
3. David E Goldberg, Genetic Algorithms.
4. John Yen and Reza Langari, Fuzzy logic Intelligence, Control, and Information, Pearson Education, Indian Edition, 2003.

References:

1. M.T.Hagan, H. B. Demuth and M. Beale, Neural Network Design, Indian reprint, 2008.
2. Fredric M.Ham and Ivica Kostanic, Principles of Neurocomputing for science and Engineering, McGraw Hill, 2001.
3. N.K. Bose and P.Liang, Neural Network Fundamentals with Graphs, Algorithms and Applications, Mc - Graw Hill, Inc. 1996.
4. Yung C. Shin and Chengying Xu, Intelligent System - Modeling, Optimization and Control, CRC Press, 2009.
5. N.K.Sinha and Madan M Gupta, Soft computing & Intelligent Systems - Theory & Applications, Indian Edition, Elsevier, 2007.
6. Witold Pedrycz, Fuzzy Control and Fuzzy Systms, Overseas Press, Indian Edition, 2008.

Academic Year 2016-17

16MES111- SENSORS AND ACTUATORS
(Elective – III)

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem

Prerequisite: None

Course Objectives:
1. To Learn about Electro mechanical sensors.
2. To Learn the use of the thermal sensors and magnetic sensors for embedded system.
3. To learn the basics of radiation sensors, smart sensors and actuators.

Course Outcomes:
1. Students will gain knowledge to interface various sensors and actuators in embedded applications.

UNIT - I: Sensors / Transducers:
Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization. **Mechanical and Electromechanical Sensors:** Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges - Inductive Sensors: Sensitivity and Linearity of the Sensor – Types-Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors.

UNIT – II: Thermal Sensors
Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermo-sensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermo-emf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors. NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors.
Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors – Anisotropic Magnetoresistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors – Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros – Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors.

UNIT - III: Radiation Sensors
Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors. **Electro analytical Sensors:** Introduction – The Electrochemical Cell – The Cell Potential - Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media.

UNIT - IV: Smart Sensors:
Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation. **Sensors –Applications:** Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring.

UNIT - V: Actuators
Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators. Mechanical Actuation Systems - Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection. Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors.

TEXT BOOKS:
1. D. Patranabis – "Sensors and Transducers" –PHI Learning Private Limited.
2. W. Bolton – "Mechatronics" –Pearson Education Limited.

REFERENCE BOOKS:
1. "Sensors, Actuators, and Their Interfaces: A Multidisciplinary Introduction", Nathan Ida, SciTech Publishing Inc (15 June 2011).
2. "Sensors and Actuators: Engineering System Instrumentation, Second Edition", **Dr. Clarence W. de Silva**, CRC Press; 2 edition (10 August 2015).

Academic Year 2016-17

16MES112 - EMBEDDED REAL TIME OPERATING SYSTEMS (Elective-IV)

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem
Prerequisite: Computer Organization and Operating System

Course Objectives:

1. To provide broad understanding of the requirements of Real Time Operating Systems.
2. To make the student understand, applications of these Real Time features using case studies.

Course Outcomes:

1. Be able to explain real-time concepts such as preemptive multitasking, task priorities, priority inversions, mutual exclusion, context switching, and synchronization, interrupt latency and response time, and semaphores.
2. Able describe how a real-time operating system kernel is implemented.
3. Able explain how tasks are managed.
4. Explain how the real-time operating system implements time management.
5. Discuss how tasks can communicate using semaphores, mailboxes, and queues.
6. Be able to implement a real-time system on an embedded processor.
7. Be able to work with real time operating systems like RT Linux, Vx Works, MicroC /OS-II, Tiny Os

UNIT – I: Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II: Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.

UNIT - III: Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV: Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V: Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOKS:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011
2. Unix Concepts and Applications, Sumitabha Das, 4th Edition , TMH.

REFERENCE BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

Academic Year 2016-17

16MES113-ADVANCED COMPUTER ARCHITECTURE

(Elective – IV)

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem (Embedded Systems)
Prerequisite: Computer Organization and Operating System

Course Objectives:

1. Explains instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
2. Explains different classifications of instruction set architectures
3. Explains the advanced concepts such as instruction level parallelism, , out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction
4. Examine software support for ILP, including VLIW and similar approaches
5. Teach memory hierarchy design issues, including caching and virtual memory approaches
6. Explains multiprocessor and parallel processing architectures
7. Gives the organization and design of contemporary processor architectures
8. As the current trend in computer architecture is towards chip-multiprocessing, the architecture of shared memory multiprocessors and chip level interconnect (network-on-chip) will be covered as future scope.

Course Outcomes:

A student who has met the objectives of the course will be able to:

1. Understand advanced computer architecture aspects
2. Describe and explain instruction level parallelism with static scheduling, out-of-order execution and network-on-chip architectures
3. Understand the architecture and limitations of chip-multiprocessing
4. Explain in detail about time-predictable computer architecture
5. Understand the operation of modern CPUs including pipelining, memory systems and busses.
6. Design and emulate a single cycle or pipelined CPU by given specifications using Hardware Description Language (HDL).
7. Write reports and make presentations of computer architecture projects

UNIT- I: Fundamentals of Computer Design:

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II: Pipelines:

Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties. **Memory Hierarchy Design:** Introduction, review of ABC of cache, Cache performance , Reducing cache miss penalty, Virtual memory.

UNIT - III: Instruction Level Parallelism the Hardware Approach:

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV: Multi Processors and Thread Level Parallelism

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V: Inter Connection and Networks:

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. **Intel Architecture:** Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.
2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs., MC Graw Hill.,

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Advanced Computer Architecture - A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk ,Pearson ed.

Academic Year 2016-17

16MES114- SCRIPTING LANGUAGES
(Elective – IV)

L	T	P	C
4	-	-	4

M.Tech. I Year I-Sem (Embedded Systems)

Prerequisite: C Language Programs

Course Objectives:
The goal of the course is to study:
1. The principles of scripting languages.
2. Motivation for and applications of scripting.
3. Difference between scripting languages and non- scripting languages.
4. Types of scripting languages.
5. Scripting languages such as PERL, TCL/TK, python and BASH.
6. Creation of programs in the Linux environment.
7. Usage of scripting languages in IC design flow.

Course Outcomes:
Upon learning the course, the student will have the:
1. Ability to create and run scripts using PERL/TCl/Python in IC design flow.
2. Ability to use Linux environment and write programs for automation of scripts in VLSI tool design flow.

Unit – 1 : Linux Basics:
Introduction to Linux , File System of the Linux, General usage of Linux kernel & basic commands, Linux users and group, Permissions for file, directory and users, searching a file & directory, zipping and unzipping concepts.

Unit – 2 : Linux Networking:
Introduction to Networking in Linux, Network basics & Tools, File Transfer Protocol in Linux, Network file system, Domain Naming Services, Dynamic hosting configuration Protocol & Network information Services.

Unit – 3 : Perl Scripting:
Introduction to Perl Scripting, working with simple values, Lists and Hashes, Loops and Decisions, Regular Expressions, Files and Data in Perl Scripting, References & Subroutines, Running and Debugging Perl, Modules, Object – Oriented Perl.

Unit – 4 : Tcl / Tk Scripting:
Tcl Fundamentals, String and Pattern Matching, Tcl Data Structures, Control Flow Commands, Procedures and Scope, Evel, Working with Unix, Reflection and Debugging, Script Libraries, Tk Fundamentals, Tk by examples, The Pack Geometry Manager, Binding

Commands to X Events, Buttons and Menus, Simple Tk Widgets, Entry and List box Widgets Focus, Grabs and Dialogs.

Unit – 5 : Python Scripting:
Introduction to Python, using the Python Interpreter, More Control Flow Tools, Data Structures, Modules, Input and Output, Errors and Exceptions, Classes, Brief Tour of the Standard Library.

Text Books:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Red Hat Enterprise Linux 4 : System Administration Guide Copyright, 2005 Red Hat Inc.

Reference Books:

1. Learning Python – 2nd Ed., Mark Lutz and David Ascher, 2003, O'Reilly.
2. Learning Perl – 4th Ed. Randal Schwartz, Tom Phoenix and Brain d foy. 2005.
3. Jython Essentials – Samuele Pedroni and Noel Pappin.2002. O'Reilly.
4. Python Tutorial by Guido Van Rossum, Fred L. Drake Jr. editor , Release 2.6.4
5. Practical Programming in Tcl and Tk by Brent Welch, Updated for Tcl 7.4 and Tk 4.0.

Academic Year 2016-17

16MES1L1- EMBEDDED SYSTEMS LABORATORY

L	T	P	C
-	-	4	2

M.Tech. I Year I-Sem

Course Objectives:

1. To make the student understand practical importance of Real Time Operating Systems.
2. To make the student understand, applications of these Real Time features through programs.
3. To make the student familiarize with an embedded platform based on Raspberry-Pi and its various applications

Course Outcomes:

1. Be able to write programs based on real-time concepts such as multitasking, task priorities and interrupt handler.
2. Be able to write programs on how tasks can communicate using semaphores and queues.
3. Be able to design a new project on embedded platform using PYTHON Programming language
4. Be able to use the interfaces of Raspberry-Pi development board

Note: Minimum of 7 experiments from Part I and 3 experiments from Part II have to be conducted.

Part -I:

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment:

Using ARM Tool chain and Library

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which
illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher
priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.

Part -II

The following experiments have to be tested using **Raspberry Pi** Development board using **PYTHON** programming language on LINUX operating system.

1. **Functional Testing Of Devices:** Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems:** Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming:** Programming of available GPIO pins of the corresponding device using Python programming language. Interfacing of I/O devices like LED/Switch/Ultrasonic sensor/PIR senor and testing the functionality.
4. **ON/OFF Control Based On Light Intensity:** Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
5. **Porting Openwrt To the Device:** Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.

Academic Year 2016-17

16MES201- SYSTEM ON CHIP ARCHITECTURE

L	T	P	C
4	-	-	4

M.Tech. I Year II-Sem

Prerequisite: Embedded System Design.

Course Objectives:
1) To introduce the architectural features of system on chip.
2) To provides information on interconnection necessities between computational block and memory block.

Course Outcomes:
1) Introduction to SOC Architecture and design.
2) Processor design Architectures and limitations
3) To acquires the knowledge of memory architectures on SOC.
4) To understands the interconnection strategies and their customization on SOC.

UNIT – I: Introduction to the System Approach:
System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II: Processors:
Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III: Memory Design for SOC:
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I , and D – Caches , Multilevel Caches, Virtual to real translation , SOC Memory System , Models of Simple Processor – memory interaction.

UNIT - IV: Interconnect Customization and Configuration:
Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V: Application Studies / Case Studies:

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JEPG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip by Michael J. Flynn and Wayne Luk, Wiely India (P) Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Eed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

Academic Year 2016-17

16MES202- EMBEDDED PROGRAMMING

M.Tech. I Year II-Sem

L	T	P	C
4	-	-	4

Prerequisite: C Language Programs

Course Objectives:

1. To explore the difference between general purpose programming languages and Embedded Programming Language.
2. To provide case studies for programming in Embedded systems.

Course Outcomes:

1. Expected to learn the basics of Embedded C with reference to 8051.
2. Understand how to handle control and data pins at hardware level.
3. Capable of introducing into objective nature of Embedded C.
4. Understand the specifications of real time embedded programming with case studies.

UNIT – I: Programming Embedded Systems in C:

Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family: Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions.

UNIT – II: Reading Switches:

Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions.

UNIT – III: Adding Structure to your Code:

Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions.

UNIT – IV: Meeting Real-Time Constraints:

Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V: Case Study: Intruder Alarm System:

Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Embedded C by **Michael J. Pont** , A Pearson Education,2002
2. The 8051 Microcontroller and Embedded Systems by Muhammad Ali Mazidi, Janice Gillispie, McKinlay and Rolin D, Pearson Education, 2006.

REFERENCE BOOKS:

1. Michael Barr, "Programming Embedded Systems in C and C++", 1st edition, O'Reilly Publishers, 1999.
2. PIC micro MCU C-An introduction to programming, The Microchip PIC in CCS C By Nigel Gardner.

Academic Year 2016-17

16MES203- DESIGN OF FAULT TOLERANT SYSTEMS
(Elective – V)

L	T	P	C
4	-	-	4

M.Tech. I Year II-Sem

Prerequisite: Digital System Design with PLDS

Course Objectives:

1. To provide or broad understanding of fault diagnosis and tolerant design Approach.
2. To illustrate the framework of test pattern generation using semi and full automatic approach.

Course Outcomes:

1. To acquire the knowledge of fundamental concepts in fault tolerant design.
2. Design requirements of self check-in circuits
3. Test pattern generation using LFSR
4. Design for testability rules and techniques for combinational circuits
5. Introducing scan architectures.
6. Design of built-in-self test.

UNIT-I: Fault Tolerant Design:

Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits. **Fault Tolerant Design:** Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts.

UNIT-II: Self Checking circuits & Fail safe Design:

Self Checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code. **Fail Safe Design:** Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design.

UNIT-III: Design for Testability:

Design for testability for combinational circuits: Basic concepts of Testability, Controllability and Observability, The Reed Muller's expansion technique, use of control and syndrome testable designs. **Design for testability by means of scan:** Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.

UNIT-IV: Logic Built-in-self-test:

BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures -BIST related terminologies, A centralized and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results.

UNIT-V: Standard IEEE Test Access Methods:

Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure -One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language.

TEXTBOOKS:

1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala, 1984,PHI
2. Digital System Test and Testable Design using HDL models and Architectures - Zainalabedin Navabi, Springer International Edition.

REFERENCES:

1. Digital Systems Testing and Testable Design-Miron Abramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books
2. Essentials of Electronic Testing- Bushnell & Vishwani D.Agarwal,Springers.
3. Design for Test for Digital IC's and Embedded Core Systems- Alfred L. Crouch, 2008, Pearson Education.

Academic Year 2016-17

16MES204- EMBEDDED NETWORKS

(Elective – V)

L	T	P	C
4	-	-	4

M.Tech. I Year II-Sem

Prerequisite: Computer Networks.

Course Objectives:

1. To elaborate on the conceptual frame work of physical layer and topological issues of networking in Embedded Systems.
2. To emphasis on issues related to guided and unguided media with specific reference to Embedded device level connectivity.

Course Outcomes :

1. Expected to acquire knowledge on communication protocols of connecting Embedded Systems.
2. Expected to master the design level parameters of USB and CAN bus protocols.
3. Understand the design issues of Ethernet in Embedded networks.
4. Acquire the knowledge of wireless protocols in Embedded domain.

UNIT –I: Embedded Communication Protocols:

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols - Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT –II: USB and CAN Bus:

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III: Ethernet Basics:

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV: Embedded Ethernet:

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V: Wireless Embedded Networking:

Wireless sensor networks – Introduction – Applications – Network Topology – Localization – Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari , Cambridge press 2005.

Academic Year 2016-17

16MES205- IMAGE AND VIDEO PROCESSING
(Elective - V)

L	T	P	C
4	-	-	4

M.Tech. I Year II-Sem

Prerequisite: Digital Image Processing

Course Objectives:

1. The student will be able to understand the quality improvement methods of Image.
2. To study the basic digital image and video filter operations.
3. Understand the fundamentals of Image Compression.
4. Understand the representation of video.
5. Understand the principles and methods of motion estimation.

Course Outcomes:

1. The students will learn image representation, filtering, compression.
2. Students will learn the basics of video processing , representation, motion estimation.

UNIT – I: Fundamentals of Image Processing and Image Transforms:
Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels. **Image Segmentation:** Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT – II: Image Enhancement: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters. **Frequency domain methods**: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

UNIT – III: Image Compression: Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, , Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT - IV: Basic Steps of Video Processing: Analog Video, Digital Video. Time-Varying Image Formation models: Three -Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT – V: 2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Digital Image Processing – Gonzaleze and Woods, 3rd ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFRENCE BOOKS:

1. Digital Video Processing – M. Tekalp, Prentice Hall International
2. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar–TMH, 2009

Academic Year 2016-17

16MES206- HARDWARE - SOFTWARE CO-DESIGN
(Elective – VI)

L	T	P	C
4	-	-	4

M.Tech. I Year II-Sem

Prerequisite: Advanced Computer Architecture , Embedded System Design**.**

Course Objective:

1. To provide a broad understanding of the specific requirement of Hardware and soft ware integration for embedded system

Course Outcomes:

1. To acquire the knowledge on various models.
2. To explore the interrelationship between Hardware and software in a embedded system.
3. Acquire the knowledge of firmware development process and tools.
4. Understand validation methods and adaptability.

UNIT –I: Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co- Synthesis Algorithms:** Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II: Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III: Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV: Design Specification and Verification:

Design, co-design, the co- design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V: Languages for System – Level Specification and Design-I:
System – level specification, design representation for system level synthesis, system level specification languages. **Languages for System – Level Specification and Design-II:** Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:
1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:
1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer
2. Embedded System Design: A Unified Hardware/Software Approach ‰ Frank Vahid and Tony Givargis, 1999

Academic Year 2016-17

16MES207- AD-HOC AND WIRELESS SENSOR NETWORKS
(Elective - VI)

L	T	P	C
4	-	-	4

M.Tech. I Year II-Sem

Prerequisite: Wireless Sensor Networks.

Course Objectives:

1. To study the fundamentals of wireless Ad-Hoc Networks.
2. To study the operation and performance of various Ad-hoc wireless network protocols.
3. To study the architecture and protocols of Wireless sensor networks.

Course Outcomes:

1. Students will be able to understand the basis of Ad-hoc wireless networks.
2. Students will be able to understand design, operation and the performance of MAC layer protocols, routing protocols and transport layer protocols of Adhoc wireless networks.
3. Students will be able to understand sensor network Architecture and will be able to distinguish between protocols used in Adhoc wireless network and wireless sensor networks.

UNIT - I: Wireless LANs and PANs:
Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF. **AD HOC WIRELESS NETWORKS:** Introduction, Issues in Ad Hoc Wireless Networks.

UNIT - II: MAC Protocols:
Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT - III: Routing Protocols:
Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT – IV: Transport Layer Protocols:
Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT – V: Wireless Sensor Networks:

Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

TEXT BOOKS:

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.

REFERENCE BOOKS:

1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C.K. Toh , 1st Ed. Pearson Education.
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer.

Academic Year 2016-17

16MES208- DIGITAL SIGNAL PROCESSORS AND CONTROLLERS
(Elective – VI)

L	T	P	C
4	-	-	4

M.Tech. I Year II-Sem

Prerequisite: Microprocessors and Micro Controllers

Course Objectives:

1. To provide a comprehensive understanding of various programs of DSP Processors.
2. To distinguish between the architectural difference of ARM and DSPs along with floating point capabilities.

Course Outcomes: The students are

1. Expected to learn various DSPs and their architectural features.
2. Explore the ARM development towards the functional capabilities of DS Processing.
3. Expected to work with ASM level program using the instruction set.
4. To explore the selection criteria of DSP / ARM processors by understanding the functional level trade off issues.

UNIT-I: Introduction to Digital Signal Processing:

Introduction, A digital Signal – Processing system, the sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation. **Architectures for Programmable DSP devices:** Basic Architectural features, DSP computational building blocks, Bus Architecture and Memory, Data addressing capabilities, Address generation UNIT, programmability and program execution, speed issues, features for external interfacing.

UNIT-II: Programmable Digital Signal Processors:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX processors, memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, On-Chip peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX processors.

UNIT-III: Architecture of ARM Processors:

Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behavior of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence. **Technical Details of ARM Processors:** General information about Cortex-M3 and cortex M4 processors-Processor type, processor

architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT-IV:

Instruction SET: Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT-V: Floating Point Operations: About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. **ARM Cortex-M4 and DSP Applications:** DSP on a microcontroller, Dot Product example, writing optimized DSP code for the Cortex-M4-Biquad filter, Fast Fourier transform, FIR filter.

TEXTBOOKS:

1. Digital Signal Processing- Avtar Singh and S. Srinivasan, Thomson Publications,2004.
2. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu, Elsevier Publications, Third edition.

REFERENCES:

1. ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004.
2. The Designers' Guide to the CORTEX-M Processor Family, Trevor Martin,

Academic Year 2016-17

16MES209- MODERN CONTROL THEORY
(Elective – VI)

L	T	P	C
4	-	-	4

M.Tech. I Year II-Sem

Prerequisite: Control Systems

Course Objectives:

1. To explain the concepts of basics and modern control system for the real time analysis and design of control systems.
2. To explain the concepts of state variables analysis.
3. To study and analyze non linear systems.
4. To analyze the concept of stability for nonlinear systems and their categorization.
5. To apply the comprehensive knowledge of optimal theory for Control Systems.

Course Outcomes: Upon completion of this course, students should be able to:

1. Various terms of basic and modern control system for the real time analysis and design of control systems.
2. To perform state variables analysis for any real time system.
3. Apply the concept of optimal control to any system.
4. Able to examine a system for its stability, controllability and Observability.
5. Implement basic principles and techniques in designing linear control systems.
6. Formulate and solve deterministic optimal control problems in terms of performance indices.
7. Apply knowledge of control theory for practical implementations in engineering and network analysis.

UNIT I: Mathematical Preliminaries and State Variable Analysis:

Fields, Vectors and Vector Spaces – Linear combinations and Bases – Linear Transformations and Matrices – Scalar Product and Norms – Eigen values, Eigen Vectors and a Canonical form representation of Linear systems – The concept of state – State space model of Dynamic systems – Time invariance and Linearity – Non uniqueness of state model

– State diagrams for Continuous-Time State models - Existence and Uniqueness of Solutions to Continuous-Time State Equations – Solutions of Linear Time Invariant Continuous-Time State Equations – State transition matrix and it's properties. Complete solution of state space model due to zero input and due to zero state.

UNIT II: Controllability and Observability:

General concept of controllability – Controllability tests, different state transformations such as diagonalization, Jordon canonical forms and Controllability canonical forms for Continuous-Time Invariant Systems – General concept of Observability – Observability tests for Continuous-Time Invariant Systems – Observability of different State transformation forms.

UNIT III: State Feedback Controllers and Observers:

State feedback controller design through Pole Assignment, using Ackkermans formula– State observers: Full order and Reduced order observers.

UNIT IV: Non-Linear Systems:

Introduction – Non Linear Systems - Types of Non-Linearities – Saturation – Dead-Zone - Backlash – Jump Phenomenon etc; Linearization of nonlinear systems, Singular Points and its types– Describing function–describing function of different types of nonlinear elements, – Stability analysis of Non- Linear systems through describing functions. Introduction to phase-plane analysis, Method of Isoclines for Constructing Trajectories, Stability analysis of nonlinear systems based on phase-plane method.

UNIT V: Stability Analysis:

Stability in the sense of Lyapunov, Lyapunov's stability and Lypanov's instability theorems - Stability Analysis of the Linear continuous time invariant systems by Lyapunov second method – Generation of Lyapunov functions – Variable gradient method – Krasooviski's method.

TEXT BOOKS:

1. M.Gopal, "Modern Control System Theory", New Age International - 1984
2. Ogata. K, "Modern Control Engineering", Prentice Hall - 1997

REFERENCES:

1. Donald E.Kirk, "Optimal Control Theory an Introduction", Prentice - Hall Network series - First edition.
2. N K Sinha, "Control Systems", New Age International – 3rd edition.

Academic Year 2016-17

16MES210- OPTIMIZATION TECHNIQUES
(Elective- VII)

M.Tech. I Year II-Sem

L	T	P	C
4	-	-	4

Prerequisite: None

Course Objectives:

1. To understand the theory of optimization methods and algorithms developed for solving various types of optimization problems.
2. To develop an interest in applying optimization techniques in problems of Engineering and Technology.
3. To apply the mathematical results and numerical techniques of optimization theory to concrete Engineering problems.

Course Outcomes: Upon the completion of this course, the student will be able to

1. Know basic theoretical principles in optimization
2. formulate optimization models and obtain solutions for optimization;
3. apply methods of sensitivity analysis and analyze post processing of results

UNIT – I: Introduction and Classical Optimization Techniques:
Statement of an Optimization problem – design vector – design constraints – constraint surface – objective function – objective function surfaces – classification of Optimization problems. **Classical Optimization Techniques:** Single variable Optimization – multi variable Optimization without constraints – necessary and sufficient conditions for minimum/maximum – multivariable Optimization with equality constraints. Solution by method of Lagrange multipliers – multivariable Optimization with inequality constraints – Kuhn – Tucker conditions.

UNIT – II: Linear Programming:
Standard form of a linear programming problem – geometry of linear programming problems – definitions and theorems – solution of a system of linear simultaneous equations – pivotal reduction of a general system of equations – motivation to the simplex method – simplex algorithm.

UNIT – III: Transportation Problem:
Finding initial basic feasible solution by north – west corner rule, least cost method and Vogel's approximation method – testing for optimality of balanced transportation problems. **Unconstrained Nonlinear Programming:** One – dimensional minimization methods: Classification, Fibonacci method and Quadratic interpolation method.

U**NIT – IV: Unconstrained Optimization Techniques:**
Uni-variate method, Powell's method and steepest descent method. **Constrained Nonlinear Programming:** Characteristics of a constrained problem, Classification, Basic approach of Penalty Function method; Basic approach of Penalty Function

method; Basic approaches of Interior and Exterior penalty function methods. Introduction to convex Programming Problem.

UNIT – V: Dynamic Programming:

Dynamic programming multistage decision processes – types – concept of sub optimization and the principle of optimality – computational procedure in dynamic programming – examples illustrating the calculus method of solution - examples illustrating the tabular method of solution.

TEXT BOOKS:

1. "Engineering optimization: Theory and practice"-by S. S.Rao, New Age International (P) Limited, 3rd edition, 1998.
2. "Introductory Operations Research" by H.S. Kasene & K.D. Kumar, Springer(India), Pvt. LTd.

REFERENCES:

1 "Optimization Methods in Operations Research and systems Analysis" – by K.V. Mital and C. Mohan, New Age International (P) Limited, Publishers, 3rd edition, 1996.
2. Operations Research – by Dr. S.D.Sharma.
3. "Operations Research: An Introduction" by H.A. Taha, PHI Pvt. Ltd., 6th edition
4. Linear Programming by G. Hadley

Academic Year 2016-17

16MES211- ROBOTICS
(Elective – VII)

L	T	P	C
4	-	-	4

M.Tech. I Year II-Sem

Prerequisite:

a) Introduction to Signals, Systems & Circuits
b) Analytical Foundations of Electronics and Communication Engineering,
c) Linear Systems
d) Elements of Control

Course Objectives:

1. This introductory course is valuable for students who wish to learn about robotics through a study of industrial robot systems analysis and design.
2. This course is suited to students from engineering and science backgrounds that wish to broaden their knowledge through working on a subject that integrates multi-disciplinary technologies.

Course Outcomes: Upon the completion of this course, the student will be able to:

1. Describe the various elements that make an industrial robot system
2. Discuss various applications of industrial robot systems
3. Analyze robot manipulators in terms of their kinematics, kinetics, and control
4. Model robot manipulators and analyze their performance, through running simulations using a MATLAB-based Robot Toolbox
5. Select an appropriate robotic system for a given application and discuss the limitations of such a system
6. Program and control an industrial robot system that performs a specific task.

UNIT - I: Introduction & Basic Definitions:

History of robots-robot anatomy, Coordinate Systems , Human arm Characteristics , Cartesian , Cylindrical, Polar, coordinate frames , mapping transform.

UNIT - II: Kinematics – Inverse Kinematics:

Kinematics, Mechanical structure and notations , description of links and joints , Denavit Hatenberg notation , manipulator transformation matrix , examples inverse kinematics.

UNIT - III: Differential Motion – Statics – Dynamic Modeling

Velocity Propagation along links, manipulator Jacobian – Jacobian singularities – Lagrange Euler formulation Newton Euler formulation basics of trajectory planning.

UNIT - IV: Robot Systems : Actuators Sensors and Vision

Hydraulic and Electrical Systems Including Pumps, valves, solenoids, cylinders, stepper motors, Encoders and AC Motors Range and use of sensors, Microswitches, Resistance Transducers, Piezo-electric, Infrared and Lasers Applications of Sensors : Reed Switches, Ultrasonic, Barcode Readers and RFID – Fundamentals of Robotic vision.

UNIT - V: Robots and Applications.

Industrial Applications – Processing applications – Assembly applications, Inspection applications , Non Industrial applications.

TEXT BOOKS:

1. Robotics and Control : R.K. Mittal and I.J. Nagarath, TMH 2003.
2. Mechatronics and Robotics: Design & Applications – A. Mutanbara, 1999, CRC Press.

REFERENCE BOOKS:

1. Robotics – K.S. Fu, R.C. Gonzalez and C.S.G. Lee, 2008, TMH.
2. Introduction to Robotics – P.J. Mckerrow, ISBN: 0201182408
3. Introduction to Robotics – S. Nikv, 2001, Prentice Hall,

Academic Year 2016-17

16MES212- NETWORK SECURITY AND CRYPTOGRAPHY
(Elective – VIII)

L	T	P	C
4	-	-	4

M.Tech. I Year II-Sem

Prerequisite: None

Course Objectives:

1. Understand the basic concept of Cryptography and Network Security, their mathematical models
2. To provide deeper understanding of application to network security, threats/vulnerabilities to networks and countermeasures
3. To create an understanding of Authentication functions the manner in which Message Authentication Codes and Hash Functions works
4. To provide familiarity in Intrusion detection and Firewall Design Principles

Course Outcomes: After completion of this course, the student shall be able to:

1. Describe computer and network security fundamental concepts and principles
2. Identify and assess different types of threats, malware, spyware, viruses, vulnerabilities
3. Encrypt and decrypt messages using block ciphers
4. Describe the inner-workings of today's remote exploitation and penetration techniques
5. Describe the inner-workings of popular encryption algorithms, digital signatures, certificates, anti-cracking techniques, and copy-right protections
6. Demonstrate the ability to select among available network security technology and protocols such as IDS, IPS, firewalls, SSL, SSH, IPSec, TLS, VPNs, etc.
7. Analyze key agreement algorithms to identify their weaknesses

UNIT- I: Introduction :

Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security, Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques. **Modern Techniques :** Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Block Cipher Design Principles.

UNIT- II: Encryption :

Triple DES, International Data Encryption algorithm, Blowfish, RC5, Characteristics of Advanced Symmetric block cifers. **Conventional Encryption:** Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

UNIT - III: Public Key Cryptography :
Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptograpy. **Number Theory :** Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

UNIT- IV: Message Authentication and Hash Functions:
Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs. **Hash and Mac Algorithms** MD File, Message digest Algorithm, Secure Hash Algorithm. Digital signatures and Authentication protocols: Digital signatures, Authentication Protocols, Digital signature standards. **Authentication Applications** Kerberos, Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT – V: IP Security Overview, Architecture, Authentication, Encapsulating Security Payload, Key Management. Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction. **Intruders, Viruses and Worms:** Intruders, Viruses and Related threats. **Fire Walls:** Fire wall Design Principles, Trusted systems.

TEXT BOOKS:
1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.

REFERENCE BOOKS:
1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
2. Network Security - Private Communication in a Public World by Charlie Kaufman, Radia Perlman and Mike Speciner, Pearson/PHI.
3. Principles of Information Security, Whitman, Thomson.
4. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH
5. Introduction to Cryptography, Buchmann, Springer.

Academic Year 2016-17

16MES213- MOBILE COMPUTING
(Elective – VIII)

M.Tech. I Year II-Sem

L	T	P	C
4	-	-	4

Prerequisites:

1. Computer Networks.
2. Distributed Systems OR Distributed Operating Systems OR Advanced Operating Systems

Course Objectives:

1. To make the student understand the concept of mobile computing paradigm, its novel applications and limitations.
2. To understand the typical mobile networking infrastructure through a popular GSM protocol
3. To understand the issues and solutions of various layers of mobile networks, namely MAC layer, Network Layer & Transport Layer
4. To understand the database issues in mobile environments & data delivery models.
5. To understand the ad hoc networks and related concepts.
6. To understand the platforms and protocols used in mobile environment.

Course Outcomes:

1. Able to think and develop new mobile application.
2. Able to take any new technical issue related to this new paradigm and come up with a solution(s).
3. Able to develop new ad hoc network applications and/or algorithms/protocols.
4. Able to understand & develop any existing or new protocol related to mobile environment

UNIT – I: Introduction :

Mobile Communications, Mobile Computing – Paradigm, Promises/Novel Applications and Impediments and Architecture; Mobile and Handheld Devices, Limitations of Mobile and Handheld Devices.GSM – Services, System Architecture, Radio Interfaces, Protocols, Localization, Calling, Handover, Security, New Data Services, GPRS, CSHSD, DECT.

UNIT –II: (Wireless) Medium Access Control (MAC) :

Motivation for a specialized MAC (Hidden and exposed terminals, Near and far terminals), SDMA, FDMA, TDMA, CDMA, Wireless LAN/(IEEE 802.11). **Mobile Network Layer :** IP and Mobile IP Network Layers, Packet Delivery and Handover Management, Location Management, Registration, Tunneling and Encapsulation, Route Optimization, DHCP.

UNIT –III: Mobile Transport Layer :

Conventional TCP/IP Protocols, Indirect TCP, Snooping TCP, Mobile TCP, Other Transport Layer Protocols for Mobile Networks. **Database Issues :** Database

Hoarding & Caching Techniques, Client-Server Computing & Adaptation, Transactional Models, Query processing, Data Recovery Process & QoS Issues.

UNIT IV: Data Dissemination and Synchronization :
Communications Asymmetry, Classification of Data Delivery Mechanisms, Data Dissemination, Broadcast Models, Selective Tuning and Indexing Methods, Data Synchronization – Introduction, Software, and Protocols.

UNIT V: Mobile Adhoc Networks (MANETs) :
Introduction, Applications & Challenges of a MANET, Routing, Classification of Routing Algorithms, Algorithms such as DSR, AODV, DSDV, Mobile Agents, Service Discovery. **Protocols and Platforms for Mobile Computing :** WAP, Bluetooth, XML, J2ME, JavaCard, PalmOS, Windows CE, Symbian OS, Linux for Mobile Devices, Android.

Text Books:

1. Jochen Schiller, "Mobile Communications", Addison-Wesley, Second Edition, 2009.
2. Raj Kamal, "Mobile Computing", Oxford University Press, 2007, ISBN: 0195686772

REFERENCE BOOKS:

1. The CDMA 2000 System for Mobile Communications – Vieri Vaughi, Alexander Damn Jaonvic – Pearson.
2. Adalestein - Fundamentals of Mobile & Parvasive Computing, 2008, TMH.

Academic Year 2016-17

16MES214- HIGH SPEED NETWORKS
(Elective-VIII)

M.Tech. I Year II-Sem

L	T	P	C
4	-	-	4

Prerequisite: Computer Networks

Course Objectives:

1. Understand of switching and data transmission.
2. Familiarize the students with the error correction and detection techniques.
3. Understanding of basic principles of Multiple Access, Frame Relay and ATM
4. Obtain the knowledge of Logical Addressing, Transport layer protocols, congestion control mechanism and Domain Name System
5. Gain an expertise in areas like Logical Network Design and routing protocols.

Course Outcomes: After completing this course the student is able to

1. Independently understand the basic data transmission and data link layer concepts.
2. Understand and explain error correction and detection.
3. Analyze the details of network layer protocols and transport layer protocols
4. Design different types of network topologies.
5. Analyze and compare various routing protocols.

UNIT I: Switching and Data Transmission:
ISO-OSI reference model. TCP/IP reference model, Circuit-switched networks, Datagram networks, Virtual-circuit networks, Structure of a switch, Telephone network, Dial-up modems, Digital Subscriber line, Cable TV networks. **Data Link Layer-Error Detection and Correction:** Introduction, Block coding, Linear Block codes, Cyclic codes, Checksum - **Data Link Control:** Framing, Flow and Error control, Protocols, Noiseless channels, Noisy channels, HDLC, Point-to-Point Protocol.

UNIT II: Multiple Access:
Random Access, Controlled Access, Channelization – **Connecting Devices:** Connecting LANs, Backbone Networks, Virtual LANs. **High Speed Networks-Frame Relay**: Packet -Switching Networks, Frame Relay Networks – **Asynchronous Transfer Mode (ATM)** : ATM Protocol Architecture, ATM Logical Connections, ATM Cells, ATM Service Categories, ATM Adaptation Layer (AAL)- **High-Speed LANs** : The Emergence of High-Speed LANs, Ethernet, Fiber Channel, Wireless LANs.

UNIT III: Network Layer:
Logical Addressing: IPv4 Addresses, IPv6 Addresses, **Internet Protocol: I**nternetworking, IPv4, IPv6, Transition from IPv4 to IPv6 - **Network Delivery -**

Routing: Forwarding, Unicast Routing Protocols, Multicast Routing Protocols. **Transport Layer and Application Layer Protocols:** Process-to-Process delivery, User Datagram Protocol (UDP), TCP, SCTP - **Congestion control:** Data traffic, Congestion, Congestion control, Quality of Service.

UNIT IV: Domain Name System:
Name space, Domain Name Space, Distribution of Name Space, DNS in the internet, Resolution, DNS messages, E-mail. **Needs and Goals for Network Design-Analyzing Business Goals and Constraints:** Using a Top-Down Network Design Constraints, Analyzing Business Goals, Analyzing Business constraints – **Analyzing Technical Goals & Tradeoffs:** Scalability, Availability, Network Performance, Security, Manageability, Usability, Adaptability, Affordability, Making Network Design Tradeoffs – **Characterizing Network Traffic:** Characterizing Traffic Flow, Traffic Load, Traffic Behavior, Quality of Service Requirements.

UNIT V: Logical Network Design:
Designing Network Design: Hierarchical Network Design, Redundant Network Design Topologies, Modular Network Design, Designing a Campus Network Design Topology, Designing the Enterprise Edge Topology, Secure Network Design Topologies. **Designing Models for Addressing and Naming:** Guidelines for Assigning Network Layer Addresses, Using a Hierarchical Model for Assigning Addresses, Designing a Model for Naming. **Selecting Switching and Routing Protocols:** Selecting Bridging & Switching Protocols, Spanning Tree Protocol Enhancements - **Selecting Routing Protocols:** Characterizing Routing protocols, IP Routing, Novell NetWare Routing, Using Multiple Routing Protocols in an Internet work.

Text Books:

1. Data Communications and Networking, *Behrouz A. Forouzan*, Fourth Edition, Tata McGraw Hill
2. High Speed Networks and Internets – Performance and Quality of Service, *William Stallings*, Second Edition, Pearson Education.

Reference Books:

1. Guide to Networking Essentials, *Greg Tomsho,Ed Tittel, David Johnson,*Fifth Edition, Thomson.
2. Computer Networks, *Andrew S. Tanenbaum*, Fourth Edition, Prentice Hall.
3. An Engineering Approach to Computer Networking , *S.Keshav*, Pearson Education.
4. Campus Network Design Fundamentals, *Diane Teare, Catherine Paquet*, Pearson Education (CISCO Press)
5. Computer Communications Networks, Mir, Pearson Education.
6. Top-Down Network Design, *Priscilla Oppenheimer*, Second Edition, Pearson Education (CISCO Press)

Academic Year 2016-17

16MES2L1- EMBEDDED PROGRAMMING LAB

M.Tech. I Year II-Sem

L	T	P	C
-	-	4	2

Course Objectives:

1. To impart knowledge on KEIL software with emphasis on various ports of 8051 Microcontroller
2. To make the students understand the difference between software delay and hardware delay
3. To make the students understand the interface of LCD and seven segment display with 89C51 Development Board
4. To provide insight to student on the ARM based program execution for GPIO, Timer, Counter, LCD, Serial Port and SD-MMC card interface

Course Outcomes:

1. Able to verify how KEIL software can be used using various 8051 ports.
2. Able to verify the interface of LCD and Seven Segment Display using 89C51 development board
3. Able to understand and verify ARM instruction set and different modes
4. Able to verify the LCD, Serial Port and SD-MMC card interface based on ARM processor

Note: Minimum of 4 programs from Part-I and 8 programs from Part -II are to be conducted.

List of Programs:

Part I

The following programs are to be implemented using KEIL Software and to be coded in Embedded C.

1.
    a. Write a simple program to print "hello world"
    b. Write a simple program to show a delay.
2. Write a C program for counting the no of times that a switch is pressed & released.
3. Illustrate the use of port header file (port M) using an interface consisting of a keypad and liquid crystal display.
4. Write a program to create a portable hardware delay.
5.
    a. Write a C program to test loop time outs.
    b. Write a C program to test hardware based timeout loops.
6. Develop a simple EOS showing traffic light sequencing.

Part II:

89C51 Based

The following programs have to be tested on **89C51** Development board/equivalent using **Embedded C Language on KEIL IDE or Equivalent.**

1. Program to toggle all the bits of Port P1 continuously with 250 ms delay.
2. Program to interface LCD data pins to port P1 and display a message on it.
3. Program to interface seven segment display unit: Whenever a key is pressed, it should be displayed on seven segment display unit
4. Program to transmit a message from Microcontroller to PC serially using RS232.
5. Program to get analog input from Temperature sensor and display the temperature Value on LCD screen.

ARM Based

The following Programs are to be implemented on ARM Processor

6. Simple Assembly Program for
    a. Addition | Subtraction | Multiplication | Division
    b. Operating Modes, System Calls and Interrupts
    c. Loops, Branches
7. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
8. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
9. Program to demonstrates a simple interrupt handler and setting up a timer
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
12. Program to demonstrate SD-MMC Card Interface.

Academic Year 2016-17

16MES2S1- SOFT SKILLS LAB
(Activity-based)

M.Tech. I Year II-Sem

L	T	P	C
-	-	4	2

Course Objectives

1. To improve the fluency of students in English
2. To facilitate learning through interaction
3. To illustrate the role of skills in real-life situations with case studies, role plays etc.
4. To train students in group dynamics, body language and various other activities which boost their confidence levels and help in their overall personality development
5. To encourage students develop behavioral skills and personal management skills
6. To impart training for empowerment, thereby preparing students to become successful professionals

Course Outcomes

CO1. Developed critical acumen and creative ability besides making them industry- ready.
CO2. Appropriate use of English language while clearly articulating ideas.
CO3. Developing insights into Language and enrich the professional competence of the students.
CO4. Enable students to meet challenges in job and career advancement.

INTRODUCTION

- Definition and Introduction to Soft Skills – Hard Skills vs Soft Skills – Significance of Soft/Life/Self Skills – Self and SWOT Analysis ***and***

1. Exercises on Productivity Development

- Effective/ Assertive Communication Skills (Activity based)
- Time Management (Case Study)
- Creativity & Critical Thinking (Case Study)
- Decision Making and Problem Solving (Case Study)
- Stress Management (Case Study)

2. Exercises on Personality Development Skills

- Self-esteem (Case Study)
- Positive Thinking (Case Study)
- Emotional Intelligence (Case Study)
- Team building and Leadership Skills (Case Study)
- Conflict Management (Case Study)

3. Exercises on Presentation Skills

- Netiquette

- Importance of Oral Presentation – Defining Purpose- Analyzing the audience-Planning Outline and Preparing the Presentation- Individual & Group Presentation- Graphical Organizers- Tools and Multi-media Visuals
- One Minute Presentations (Warming up)
- PPT on Project Work- Understanding the Nuances of Delivery- Body Language – Closing and Handling Questions – Rubrics for Individual Evaluation (Practice Sessions)

4. Exercises on Professional Etiquette and Communication

- Role-Play and Simulation- Introducing oneself and others, Greetings, Apologies, Requests, Agreement & Disagreement….etc.
- Telephone Etiquette
- Active Listening
- Group Discussions (Case study)- Group Discussion as a part of Selection Procedure- Checklist of GDs
- Analysis of Selected Interviews (Objectives of Interview)
- Mock-Interviews (Practice Sessions)
- Job Application and Preparing Resume
- Process Writing (Technical Vocabulary) – Writing a Project Report- Assignments

5. Exercises on Ethics and Values

- Introduction — Types of Values - Personal, Social and Cultural Values - Importance of Values in Various Contexts
- Significance of Modern and Professional Etiquette – Etiquette (Formal and Informal Situations with Examples)
  - Attitude, Good Manners and Work Culture (Live Examples)
  - Social Skills - Dealing with the Challenged (Live Examples)
  - Professional Responsibility – Adaptability (Live Examples)
  - Corporate Expectations
- Note: Hand-outs are to be prepared and given to students.
- Training plan will be integrated in the syllabus.
- Topics mentioned in the syllabus are activity-based.

SUGGESTED SOFTWARE:

- The following software from **'train2success.com'**
- Preparing for being Interviewed
- Positive Thinking
- Interviewing Skills
- Telephone Skills
- Time Management
- Team Building
- Decision making

SUGGESTED READING:

1. Alex, K. 2012. Soft Skills. S. Chand Publishers
2. Management Shapers. 2011. Collection of 28 Books by different Authors. Universities Press.
3. Sherfield, Robert M. 2005. et al Cornerstone: Developing Soft Skills. Pearson
4. Suresh Kumar,E; Sreehari, P. & Savithri, J. 2011. Communication Skills and Soft Skills-An Integrated Approach. New Delhi: Pearson
5. The ACE of Soft Skills by Gopalaswamy Ramesh & Mahadevan Ramesh. 2013. Pearson Publishers. New Delhi.
6. Patnaik, P. 2011. Group Discussion and Interview Skills. New Delhi: Foundation
7. Sudhir Andrews. 2009. How to Succeed at Interviews. New Delhi: Tata McGraw Hill
8. **Sasikumar, V & Dhamija, P.V. 1993. Spoken English - A Self-Learning Guide to Conversation Practice. New Delhi: Tata McGraw-Hill**
9. Dixso, Richard J. Everyday Dialogues in English. Prentice Hall India Pvt Ltd
10. Mukhopadhyay. L et al. 2012. Polyskills. New Delhi: CUP India Pvt Ltd
11. Rizvi, M. A. 2005. Effective Technical Communication. New Delhi: Tata McGraw Hill
12. The Hindu Speaks on Education by the Hindu Newspaper
13. Naterop, B. Jean and Revell, Rod. 2004. Telephoning in English. Cambridge: CUP